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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,242	01/14/2004	James A. Bailey	Bailey 8-1-3	4363

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EXAMINER	
NGUYEN, LINH V	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,242	BAILEY ET AL.	
	Examiner	Art Unit	
	Linh V. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7 and 9-11* is/are rejected.

7)☒ Claim(s) *4,8 and 12-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application No. 10/707803 filed on 01/14/04. Claims 1 – 18 are pending on this application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 – 3, 5 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Andoh et al. U.S. patent No. 5,936,466.

Regarding claim 1, Fig. 8 and 9 of Andoh et al. discloses a circuitry comprising: a first differential transistor pair (44, 42) connected between a first load device (50) and a first current sink (37), wherein: a first inductance-creating element (52) is connected to the first load device (5) to add inductance at a first output node (41) of the circuitry; and a power-supply rejection element (60) is connected between the first inductance-creating element (52) and a first voltage reference (Ground) to provide power-supply rejection (VDD) at the first output node (41).

Regarding claim 2, Fig. 8 and 9 further comprising: a second load device (51) connected to the first differential transistor pair (42, 43); and a second inductance-creating element (53) connected to the second load device (51) to add inductance at a

second output node (40) of the circuitry, wherein the power-supply rejection element (60) is connected between the second inductance-creating element (53) and the first voltage reference to provide power-supply rejection (VDD) at the second output node (51).

Regarding claim 3, Fig. 8 and 9 further comprising a second differential transistor pair (61,62) connected between the first and second load (50, 51) devices and a second current sink (63) such that the circuitry is adapted to provide a variable-gain amplifier function (See Col. 6 lines 56 – 63).

Regarding claims 5 and 9, Fig. 8 and 9 further comprising: a common-mode sense circuit (Feed back signals, which are input signal of into 56, 57) connected to the first and second output nodes (40 – 41) and adapted to generate a sensed common-mode voltage signal (Voltage signal at the gate of 56, 57); and a differential amplifier (56 - 59) connected to receive the sensed common-mode voltage signal (Voltage at the input gates of 56, 56) and a desired common mode voltage signal (VreF) and adapted to generate and apply a common-mode error-correction signal (outputs of 56, 57) to the first and second inductance-creating elements (52, 53) to correct for differences between the sensed and the desired common-mode voltage signals (Col. 3 lines 65 – 67).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6, 7,10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andoh et al. as applied to claims 5 and 9 above, and further in view of Hamano et al.U.S. Patent No. 5,510,745.

7. Regarding claim 6 and 10, Andoh et al. as applied to claim 5 and 9 above, does not disclose a first capacitor connected between the first output node and a second reference voltage; and a second capacitor connected between the second output node and the second reference voltage such that the circuitry is adapted to provide a continuous-time filter function.

Fig. 1D of Hammano discloses a differential transistor pair (Q1, Q2) having a first capacitor (C1) connected between the first output node (I1) and a second reference voltage (Ground); and a second capacitor (C2), connected between the second output node (I2) and the second reference voltage (Ground) such that the circuitry is adapted to provide a continuous-time filter function (connection structures of C1 and C2 are providing filter function to the outputs of Q1 and Q2).

Andoh et al. and Hammano et al. are common subject matter for differential transistor pair. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated the C1 and C2 taught by Hammano et al. into Andoh et al. for the purpose of providing a filter function to the output of differential pair transistor.

8. Regarding claims 7 and 11, Andoh et al. combined with Hammano et al. as applied to claim 6 and 10 above, does not discloses C1 and C2 are variable capacitors.

Andoh et al., Col. 19 line 48 – 50 further discloses a variable capacitor to control the frequency band.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the variable capacitor taught by Andoh et al. for the purpose of providing a filter having frequency control function to the output of differential pair transistor.

Allowable Subject Matter

9. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not teach or suggests wherein when current through the first current sink increases current through the second current sink is adapted to decrease such that total current through the first and second current sinks remains substantially constant to provide the VGA function with near exponential gain control.

Claims 8 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not teach or suggests wherein the power-supply rejection element comprises a current whose current is

controlled by a control signal that is adapted to be adjusted to adjust equivalent resistance provided by the first and second inductance-creating elements.

Claims 13 - 16 and 17 - 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. With respect to claims 13 and 17, the prior art does not teach or suggests the sources of transistors M1, M2, and M3 are connected together and to receive the common-mode error-correction signal; and the gates of transistors M1, M2, and M3 and the drain of transistor M1 are connected together and to receive the current from current source I1.

Prior Art

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Contact Information

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (571) 272-1812. The fax phone numbers for the organization where this application or proceeding is assigned are

(703-872-9306) for regular communications and (703-872-9306) for After Final communications.

5/5/05

Linh Van Nguyen

Art Unit 2819